electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.5 V, I_{OH} = −400 µA	V_{IC} = −3 V to 3 V			0.5	V
				V_{IC} = −15 V to 15 V			1	
V_{IT-}	Negative-going input threshold voltage		V_O = 0.4 V, I_{OL} = 16 mA	V_{IC} = −3 V to 3 V			−0.5	V
				V_{IC} = −15 V to 15 V			−1	
V_{OH}	High-level output voltage		V_{ID} = 1 V, I_{OH} = −400 µA	$V_{(STRB)}$ = 2.1 V,	2.5	4.2	5.5	V
			V_{ID} = −1 V, I_{OH} = −400 µA	$V_{(STRB)}$ = 0.4 V,	2.5	4.2	5.5	
V_{OL}	Low-level output voltage		V_{ID} = −1 V, I_{OL} = 16 mA	$V_{(STRB)}$ = 2.1 V,		0.25	0.4	V
I_I	Input current	Inverting input	V_{IC} = 15 V			3	4.2	mA
			V_{IC} = 0			0	−0.5	
			V_{IC} = −15 V			−3	−4.2	
		Noninverting input	V_{IC} = 15 V			5	7	mA
			V_{IC} = 0			−1	−1.4	
			V_{IC} = −15 V			−7	−9.8	
$I_{IH(STRB)}$	High-level strobe input current		$V_{(STRB)}$ = 5.5 V				5	µA
$I_{IL(STRB)}$	Low-level strobe input current		$V_{(STRB)}$ = 0			−1	−1.4	mA
r_I	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		kΩ
	Line terminating resistance		T_A = 25°C		120	170	250	Ω
I_{OS}	Short-circuit output current		V_{CC} = 5.5 V,	V_O = 0	−2.8	−4.5	−6.7	mA
I_{CC}	Supply current (average per receiver)		V_{IC} = 15 V,	V_{ID} = −1 V		4.2	6	mA
			V_{IC} = 0,	V_{ID} = −0.5 V		6.8	10.2	
			V_{IC} = −15 V,	V_{ID} = −1 V		9.4	14	

† Unless otherwise noted, $V_{(STRB)} \geq 2.1$ V or open.
‡ All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low- to high-level output from differential input	R_L = 400 Ω, C_L = 15 pF, See Figure 1		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high- to low-level output from differential input			31	45	ns
$t_{PLH(S)}$	Propagation delay time, low- to high-level output from STRB input			9	30	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output from STRB input			15	25	ns

TYPICAL CHARACTERISTICS†

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

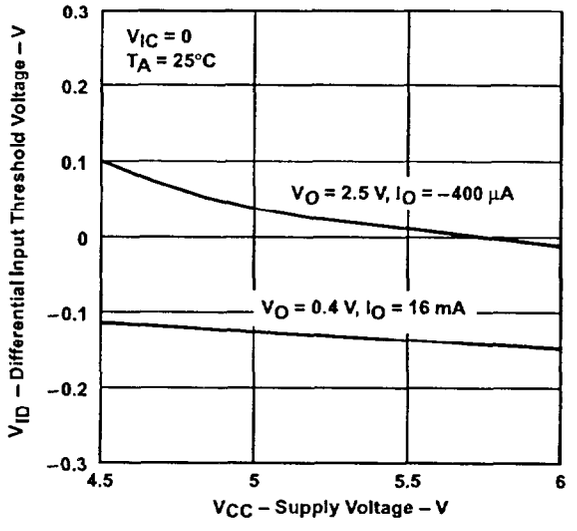

Figure 2

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

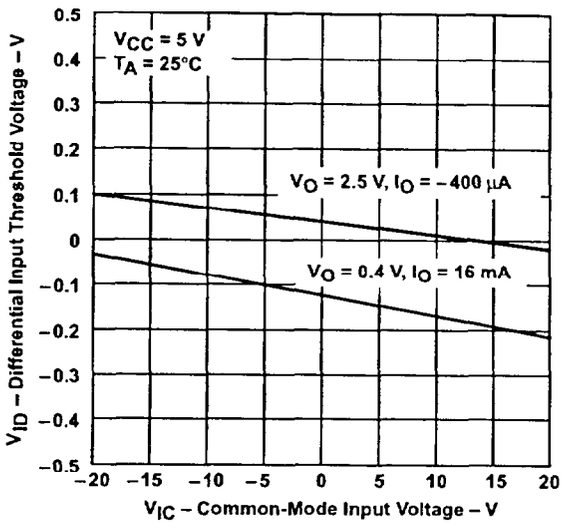

Figure 3

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

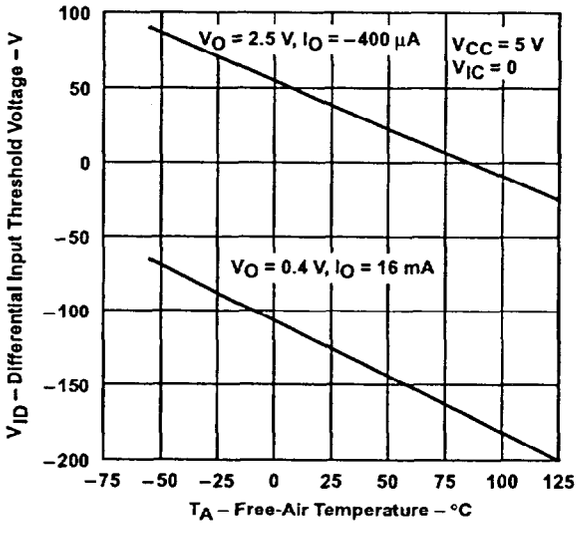

Figure 4

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

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TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

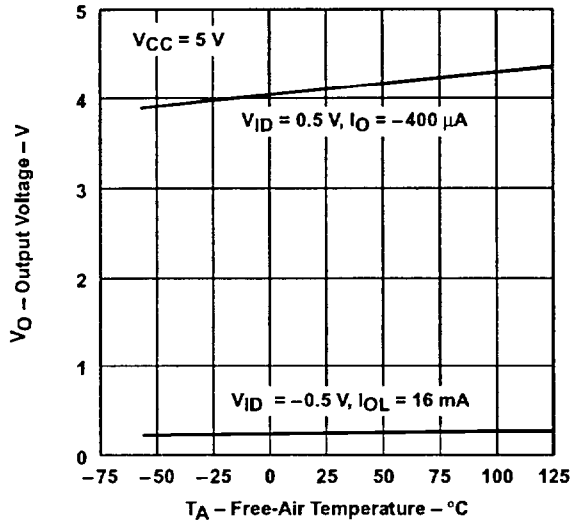


Figure 5

VOLTAGE TRANSFER CHARACTERISTICS

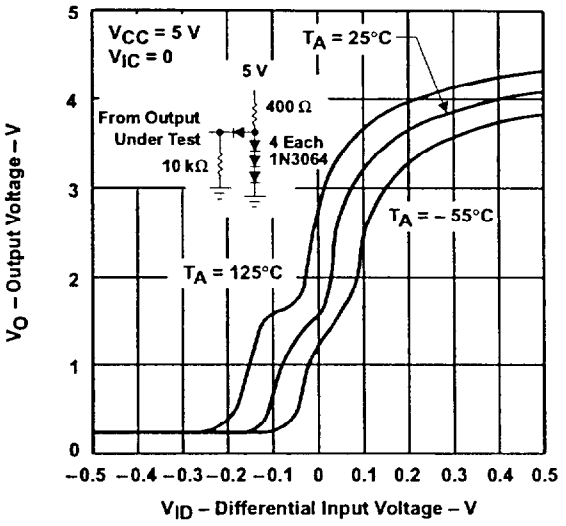


Figure 6

INPUT CURRENT
vs
INPUT VOLTAGE

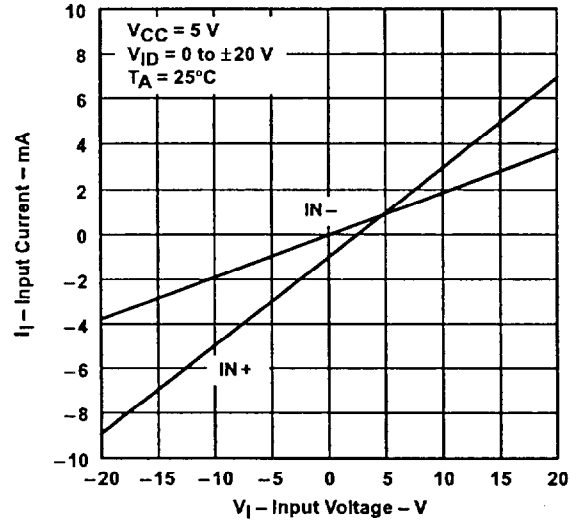


Figure 7

TERMINATING RESISTANCE
vs
FREE-AIR TEMPERATURE

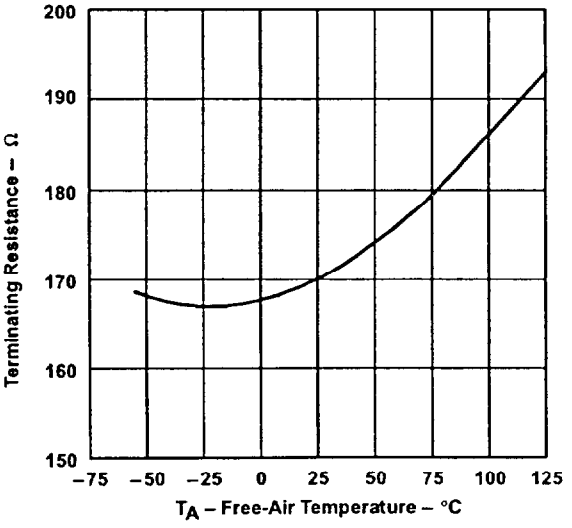
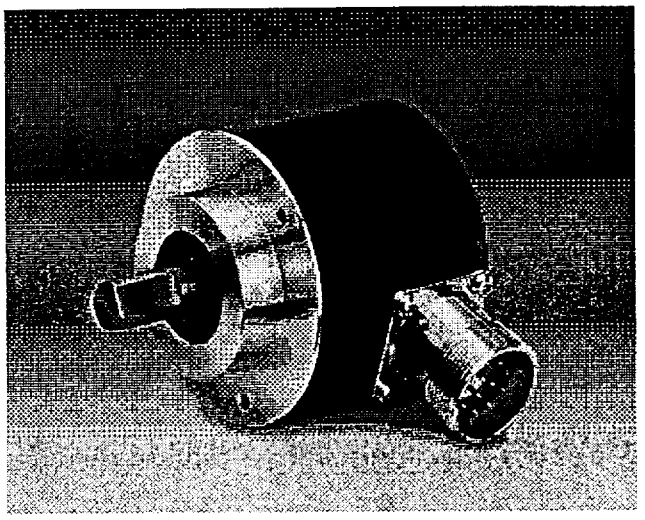


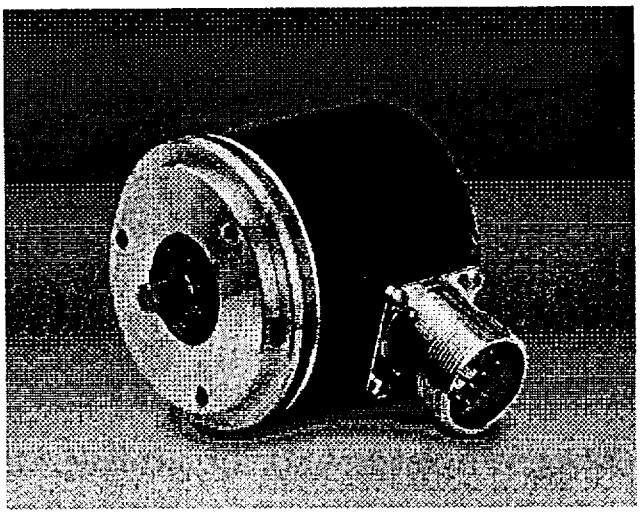
Figure 8

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

Incremental encoder



GI 355 clamping flange



GI 356 synchro flange

Features

Incremental encoder with integrated OPTO-ASIC, thus high interference immunity

Speed up to 10,000 RPM

Resolution up to 6,000 pulses
(Higher resolution up to 16,384 pulses upon request)

Signal outputs A, A inv., B, B inv., N, N inv.

Temperature range with 5 VDC up to 100 °C

Electrical data

Supply voltage	5 VDC ±10 % 10 ... 30 VDC with reverse volt. prot. 4.75 ... 30 VDC
Current consumption	Max. 60 mA (w/o load) for 24 VDC Max. 30 mA (w/o load) for 5 VDC
Max. operating frequency	150 kHz
Output signals	Channel A, B, N + inverted
Output stages	
5 VDC	Line driver to RS422
10 ... 30 VDC	Push-pull output, short-circuit-protected
4.75 ... 30 VDC	Push-pull output, short-circuit-protected
Electric connector	The electric connector must not be plugged on or removed whilst under voltage.

Mechanical data

RPM value	Max. 10,000 RPM
Starting torque	
w/o seal (IP54)	< 0.010 Nm
with seal (IP65)	< 0.015 Nm
Shaft loading	
axial	< 20 N
radial	< 40 N
Inertia torque	1.45 x 10^{-6} kgm²
Housing material	Aluminium
Weight	Approximately 250 g

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GI 355, GI 356

Order designation

Order Flange / Shaft

GI355
- 0 Clamping flange / 10 mm IP 54
- A Clamping flange / 10 mm IP 65

GI356
- 1 Synchro flange / 6 mm IP 54
- B Synchro flange / 6 mm IP 65

Voltage / Signals
- 22 5 VDC / Line driver RS422
- 60 10 ... 30 VDC push-pull output + inv.
- 70 4.75 ... 30 VDC push-pull outp. + inv.

Connection
- C2 C-plug with 12 pins, axial
- C3 C-plug with 12 pins, radial
- 31 Cable 1 m (10 ... 30 VDC) / 4.75 ... 30 VDC, axial
- 41 Cable 1 m (10 ... 30 VDC) / 4.75 ... 30 VDC, radial
- 51 Cable 1 m (5 VDC), axial
- 61 Cable 1 m (5 VDC), radial

Pulses / Order no.

Pulse	no.	Pulse	no.
5	49	500	15
10	36	1000	22
25	50	1024	23
50	39	1250	24
60	40	1500	26
100	41	2000	28
128	57	2500	30
200	06	3600	31
250	09	5000	35
360	13	6000	48
400	14		

Further pulse numbers upon request

GI 355. □□□□□□□ **clamping flange**

GI 356. □□□□□□□ **synchro flange**

Ambient conditions

Ambient temperature	-20 ... +100 °C for 5 VDC -20 ... +70 °C for 10 ... 30 VDC -20 ... +70 °C for 4.75 ... 30 VDC
Storage temperature	-20 ... +100 °C
Protection to	
Shaft w/o seal	IP 54
Shaft with seal	IP 65
Relative humidity	Max. 95 %, non condensing
Endurance	
Vibration	IEC 68, Section 2 - 6 $\leq$ 100 m/s² / 16 - 2000 Hz
Shock	IEC 68, Section 2 - 27 $\leq$ 1000 m/s² / 4 ms
Interference immunity	EN 50082-2 EN 61000-4 -2 to 4 Severity grade 3
Emitted interference	EN 50081-2

Accessories

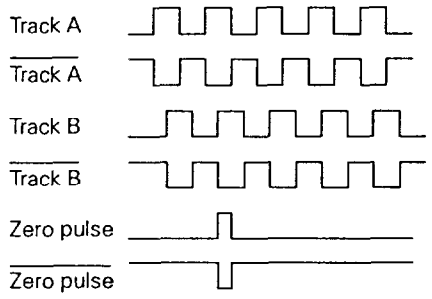
Order no.

Z 119.015	Mounting bell for synchro flange
Z 119.017	Angular fixing for clamping flange
Z 119.018	Eccentric fixing + screws
	Extension cord with connector on one side
Z 141.001	Connector without cable
Z 141.003	Connector with cable 2 m
Z 141.005	Connector with cable 5 m
Z 141.007	Connector with cable 10 m

GI 355, GI 356

Output signals

Signals with clockwise sense of rotation when looking at the flange



Line driver (5 VDC)

Level High	≥ 2.5 V	(with I = -20 mA)
Level Low	≤ 0.5 V	(with I = 20 mA)
Load High	≤ 20 mA	
Load Low	≤ 20 mA	

Push-pull output (10 ... 30 VDC)

Level High	≥ UB -3 V	(with I = -20 mA)
Level Low	≤ 1.5 V	(with I = 20 mA)
Load High	≤ 40 mA	
Load Low	≤ 40 mA	

Push-pull output (4.75 ... 30 VDC)

Level High	≥ UB -3 V	(with I = -20 mA)
Level Low	≤ 0.5 V	(with I = 20 mA)
Load High	≤ 20 mA	
Load Low	≤ 20 mA	

Pin assignment

Pin	Cable color	Assignment
1	pink	Track B inv.
2	blue	UB Sense
3	red	Track N (zero pulse)
4	black	Track N inv. (zero pulse inv.)
5	brown	Track A
6	green	Track A inv.
7	–	–
8	gray	Track B
9	–	–
10	white/green	GND
11	white	GND Sense
12	brown/green	UB

Attention: UB Sense and GND Sense are directly connected to UB and/or GND

Recommendation: Please use leads twisted in pairs for cable lengths of more than 10 m

Agilent Technologies
Innovating the HP Way

Quadrature Decoder/Counter Interface ICs

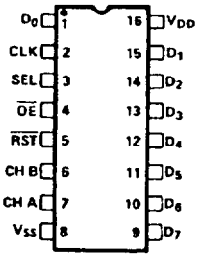
Technical Data

HCTL-2000
HCTL-2016
HCTL-2020

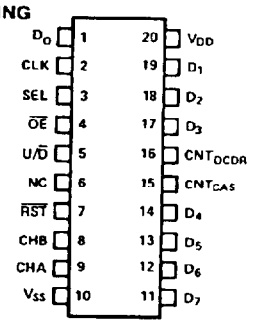
Features

- **Interfaces Encoder to Microprocessor**
- **14 MHz Clock Operation**
- **Full 4X Decode**
- **High Noise Immunity:** Schmitt Trigger Inputs Digital Noise Filter
- **12 or 16-Bit Binary Up/ Down Counter**
- **Latched Outputs**
- **8-Bit Tristate Interface**
- **8, 12, or 16-Bit Operating Modes**
- **Quadrature Decoder Output Signals, Up/Down and Count**
- **Cascade Output Signals, Up/ Down and Count**
- **Substantially Reduced System Software**

DIGITAL MOTION ENCODING



PINOUT A



PINOUT B

Applications

- **Interface Quadrature Incremental Encoders to Microprocessors**
- **Interface Digital Potentiometers to Digital Data Input Buses**

Description

The HCTL-2000, 2016, 2020 are CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-20XX family is designed to improve system performance

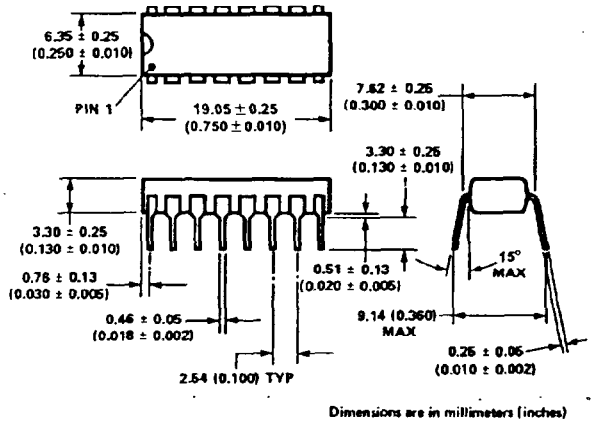
Devices

Part Number	Description	Package Drawing
HCTL-2000	12-bit counter. 14 MHz clock operation.	A
HCTL-2016	All features of the HCTL-2000. 16-bit counter.	A
HCTL-2020	All features of the HCTL-2016. Quadrature decoder output signals. Cascade output signals.	B

ESD WARNING: Standard CMOS handling precautions should be observed with the HCTL-20XX family ICs.

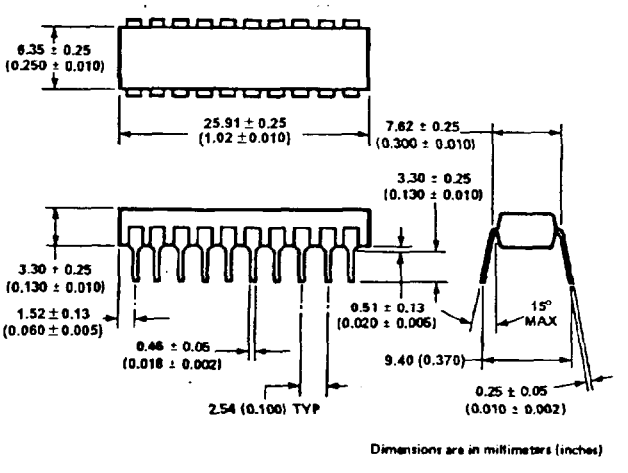
in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The entire HCTL-20XX family consists of a 4x quadrature decoder, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2000 contains a 12-bit counter. The HCTL-2016 and 2020 contain a 16-bit counter. The HCTL-2020 also contains quadrature decoder output signals and cascade signals for use with many standard counter ICs. The HCTL-20XX family provides LSTTL compatible tri-state output buffers. Operation is specified for a temperature range from -40 to +85°C at clock frequencies up to 14 MHz.

Package Dimensions



PACKAGE A LEAD FINISH: SOLDER DIPPED

PACKAGE A



PACKAGE B LEAD FINISH: SOLDER DIPPED

PACKAGE B

Operating Characteristics

Table 1. Absolute Maximum Ratings

(All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +5.5	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Storage Temperature	T_S	-40 to +125	°C
Operating Temperature	T_A[1]	-40 to +85	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	+4.5 to +5.5	V
Ambient Temperature	T_A[1]	-40 to +85	°C

Table 3. DC Characteristics V_{DD} = 5 V ± 5%; T_A = -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}[2]	Low-Level Input Voltage				1.5	V
V_{IH}[2]	High-Level Input Voltage		3.5			V
V_{T+}	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
V_{T-}	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_H	Schmitt-Trigger Hysteresis		1.0	2.0		V
I_{IN}	Input Current	$V_{IN} = V_{SS}$ or V_{DD}	-10	1	+10	µA
V_{OH}[2]	High-Level Output Voltage	I_{OH} -1.6 mA	2.4	4.5		V
V_{OL}[2]	Low-Level Output Voltage	I_{OL} = +4.8 mA		0.2	0.4	V
I_{OZ}	High-Z Output Leakage Current	$V_O = V_{SS}$ or V_{DD}	-10	1	+10	µA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{SS}$ or V_{DD}, V_O = HiZ		1	5	µA
C_{IN}	Input Capacitance	Any Input[3]		5		pF
C_{OUT}	Output Capacitance	Any Output[3]		6		pF

Notes:
1. Free air.
2. In general, for any V_{DD} between the allowable limits (+4.5 V to +5.5 V), V_{IL} = 0.3 V_{DD} and V_{IH} = 0.7 V_{DD}; typical values are $V_{OH} = V_{DD}$ - 0.5 V @ I_{OH} = -40 µA and $V_{OL} = V_{SS}$ + 0.2 V @ I_{OL} = 1.6 mA.
3. Including package capacitance.

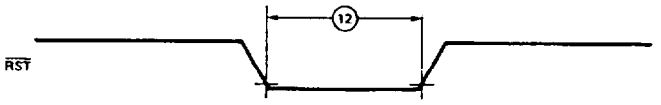


Figure 1. Reset Waveform.

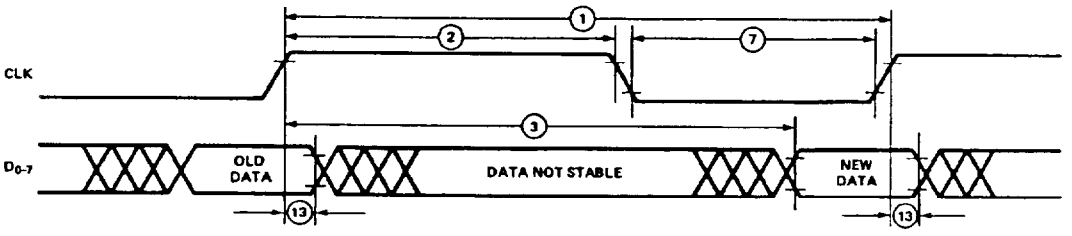


Figure 2. Waveform for Positive Clock Related Delays.

Functional Pin Description

Table 4. Functional Pin Descriptions

<table>
<tr><th>Symbol</th><th>Pin 2000/2016</th><th>Pin 2020</th><th>Description</th></tr>
<tr><td>V_{DD}</td><td>16</td><td>20</td><td>Power Supply</td></tr>
<tr><td>V_{SS}</td><td>8</td><td>10</td><td>Ground</td></tr>
<tr><td>CLK</td><td>2</td><td>2</td><td>CLK is a Schmitt-trigger input for the external clock signal.</td></tr>
<tr><td>CHA
CHB</td><td>7
6</td><td>9
8</td><td>CHA and CHB are Schmitt-trigger inputs which accept the outputs from a quadrature encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.</td></tr>
<tr><td>$\overline{RST}$</td><td>5</td><td>7</td><td>This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. $\overline{RST}$ is asynchronous with respect to any other input signals.</td></tr>
<tr><td>$\overline{OE}$</td><td>4</td><td>4</td><td>This CMOS active low input enables the tri-state output buffers. The $\overline{OE}$ and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.</td></tr>
<tr><td>SEL</td><td>3</td><td>3</td><td>This CMOS input directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in $\overline{OE}$ above, SEL also controls the internal inhibit logic.
<table>
<tr><th>SEL</th><th>BYTE SELECTED</th></tr>
<tr><td>0</td><td>High</td></tr>
<tr><td>1</td><td>Low</td></tr>
</table></td></tr>
<tr><td>CNT_{DCDR}</td><td></td><td>16</td><td>A pulse is presented on this LSTTL-compatible output when the quadrature decoder has detected a state transition.</td></tr>
<tr><td>$U/\overline{D}$</td><td></td><td>5</td><td>This LSTTL-compatible output allows the user to determine whether the IC is counting up or down and is intended to be used with the CNT_{DCDR} and CNT_{CAS} outputs. The proper signal U (high level) or $\overline{D}$ (low level) will be present before the rising edge of the CNT_{DCDR} and CNT_{CAS} outputs.</td></tr>
<tr><td>CNT_{CAS}</td><td></td><td>15</td><td>A pulse is presented on this LSTTL-compatible output when the HCTL-2020 internal counter overflows or underflows. The rising edge on this waveform may be used to trigger an external counter.</td></tr>
<tr><td>D0</td><td>1</td><td>1</td><td rowspan="8">These LSTTL-compatible tri-state outputs form an 8-bit output port through which the contents of the 12/16-bit position latch may be read in 2 sequential bytes. The high byte, containing bits 8-15, is read first (on the HCTL-2000, the most significant 4 bits of this byte are set to 0 internally). The lower byte, bits 0-7, is read second.</td></tr>
<tr><td>D1</td><td>15</td><td>19</td></tr>
<tr><td>D2</td><td>14</td><td>18</td></tr>
<tr><td>D3</td><td>13</td><td>17</td></tr>
<tr><td>D4</td><td>12</td><td>14</td></tr>
<tr><td>D5</td><td>11</td><td>13</td></tr>
<tr><td>D6</td><td>10</td><td>12</td></tr>
<tr><td>D7</td><td>9</td><td>11</td></tr>
<tr><td>NC</td><td></td><td>6</td><td>Not connected - this pin should be left floating.</td></tr>
</table>

Switching Characteristics

Table 5. Switching Characteristics Min/Max specifications at V_{DD} = 5.0 ± 5%, T_A = -40 to + 85°C.

	Symbol	Description	Min.	Max.	Units
1	t_{CLK}	Clock period	70		ns
2	t_{CHH}	Pulse width, clock high	28		ns
3	t_{CD}[1]	Delay time, rising edge of clock to valid, updated count information on D0-7		65	ns
4	t_{ODE}	Delay time, $\overline{OE}$ fall to valid data		65	ns
5	t_{ODZ}	Delay time, $\overline{OE}$ rise to Hi-Z state on D0-7		40	ns
6	t_{SDV}	Delay time, SEL valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		65	ns
7	t_{CLH}	Pulse width, clock low	28		ns
8	t_{SS}[2]	Setup time, SEL before clock fall	20		ns
9	t_{OS}[2]	Setup time, $\overline{OE}$ before clock fall	20		ns
10	t_{SH}[2]	Hold time, SEL after clock fall	0		ns
11	t_{OH}[2]	Hold time, $\overline{OE}$ after clock fall	0		ns
12	t_{RST}	Pulse width, $\overline{RST}$ low	28		ns
13	t_{DCD}	Hold time, last position count stable on D0-7 after clock rise	10		ns
14	t_{DSD}	Hold time, last data byte stable after next SEL state change	5		ns
15	t_{DOD}	Hold time, data byte stable after $\overline{OE}$ rise	5		ns
16	t_{UDD}	Delay time, $U/\overline{D}$ valid after clock rise		45	ns
17	t_{CHD}	Delay time, CNT_{DCDR} or CNT_{CAS} high after clock rise		45	ns
18	t_{CLD}	Delay time, CNT_{DCDR} or CNT_{CAS} low after clock fall		45	ns
19	t_{UDH}	Hold time, $U/\overline{D}$ stable after clock rise	10		ns
20	t_{UDCS}	Setup time, $U/\overline{D}$ valid before CNT_{DCDR} or CNT_{CAS} rise	t_{CLK}-45		ns
21	t_{UDCH}	Hold time, $U/\overline{D}$ stable after CNT_{DCDR} or CNT_{CAS} rise	t_{CLK}-45		ns

Notes:

1. t_{CD} specification and waveform assume latch not inhibited.
2. t_{SS}, t_{OS}, t_{SH}, t_{OH} only pertain to proper operation of the inhibit logic. In other cases, such as 8 bit read operations, these setup and hold times do not need to be observed.

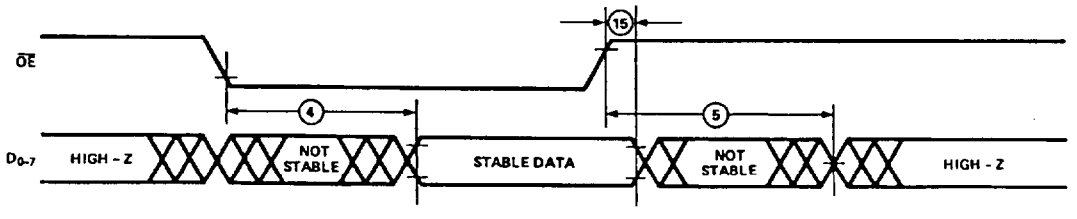


Figure 3. Tri-State Output Timing.

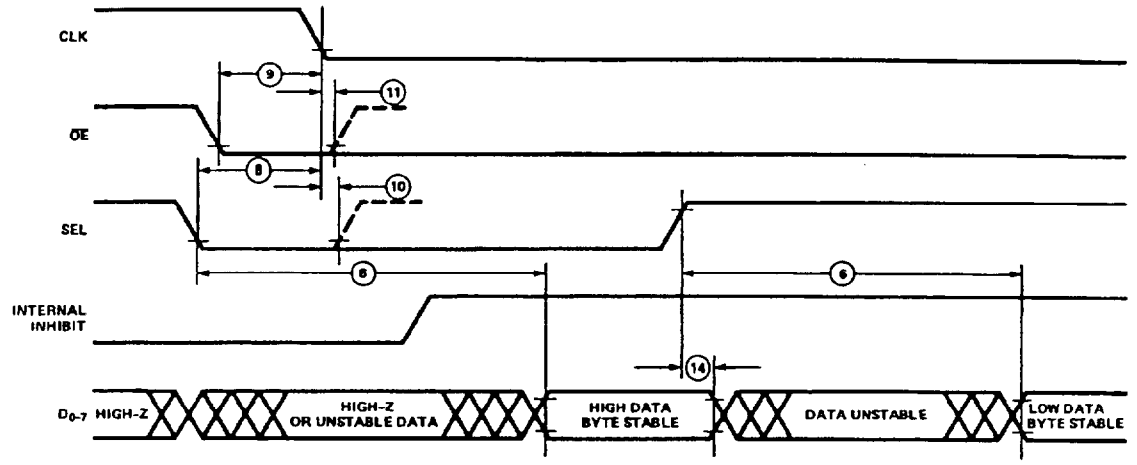


Figure 4. Bus Control Timing.

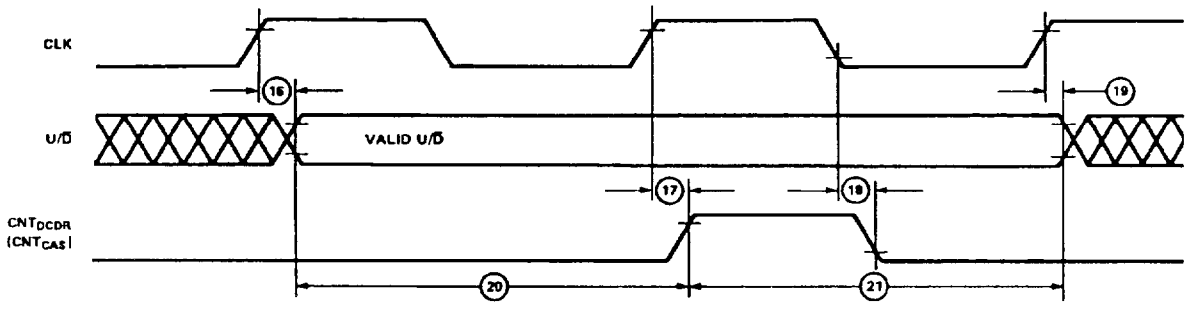


Figure 5. Decoder, Cascade Output Timing (HCTL-2020 only).

Operation

A block diagram of the HCTL-20XX family is shown in Figure 6. The operation of each major function is described in the following sections.

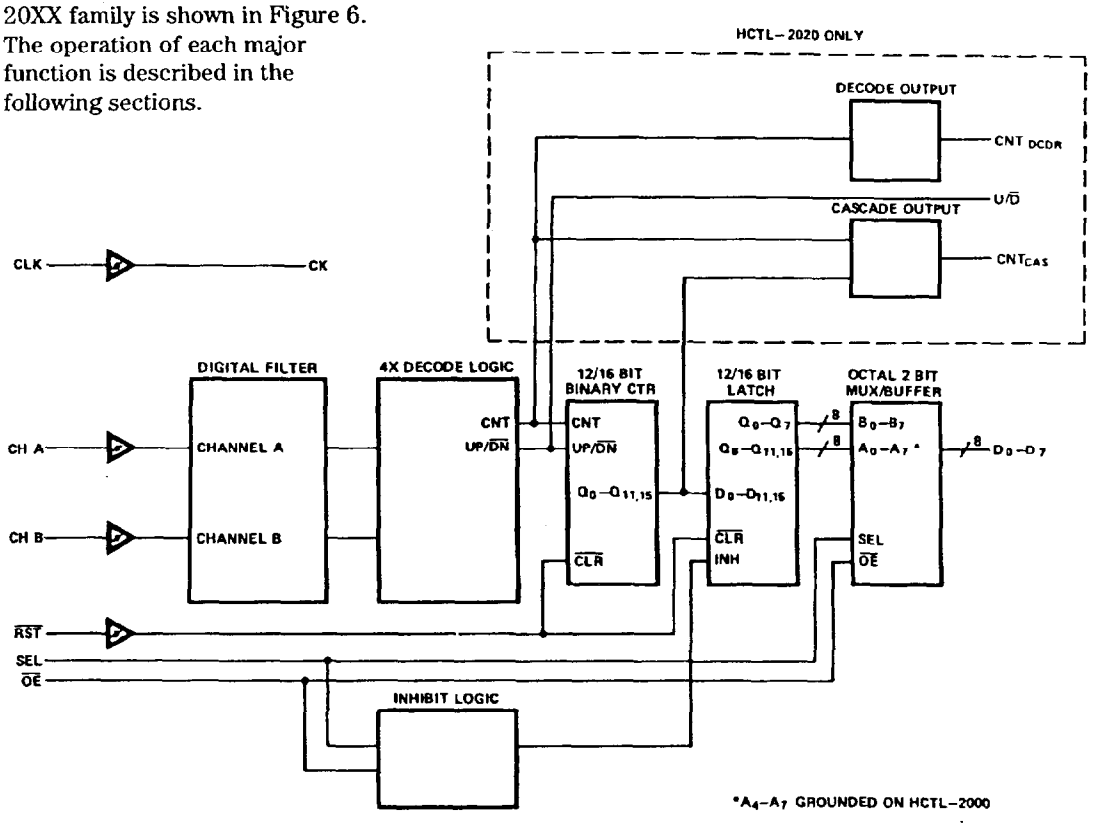


Figure 6. Simplified Logic Diagram.

Digital Noise Filter

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a three-clock-cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved integrity of the data in the counter. False counts triggered by noise are avoided.

Figure 7 shows the simplified schematic of the input section. The signals are first passed through a Schmitt trigger buffer to address the problem of input signals with slow rise times and low level noise (approximately < 1 V). The cleaned up signals are then passed to a four-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges. Refer to Figure 8 which shows the timing diagram. The result of this circuitry is that short noise spikes between rising clock edges are ignored and pulses shorter than two clock periods are rejected.

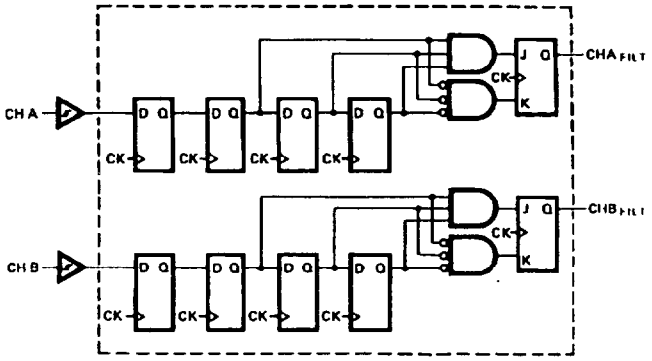


Figure 7. Simplified Digital Noise Filter Logic.

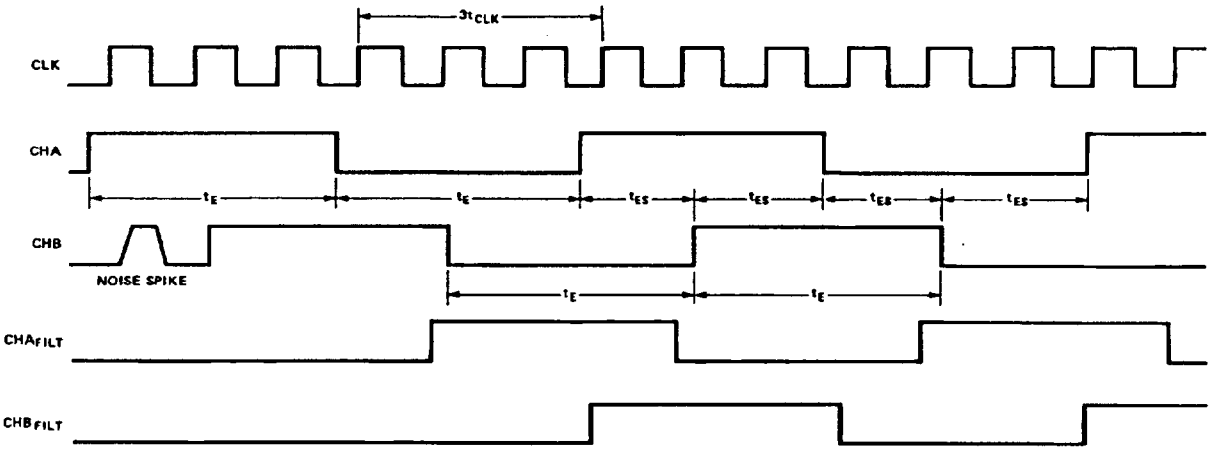


Figure 8. Signal Propagation through Digital Noise Filter.

Quadrature Decoder

The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four (4X decoding). When using an encoder for motion sensing, the user benefits from the increased resolution by being able to provide better system control.

The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the internal position counter. In the case of the HCTL-2020, the signals also go to external pins 5 and 16 respectively.

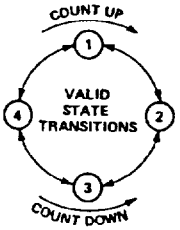
Figure 9 shows the quadrature states and the valid state transitions. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.

Design Considerations

The designer should be aware that the operation of the digital filter places a timing constraint on the relationship between incoming quadrature signals and the external clock. Figure 8 shows the timing waveform with an incremental encoder input. Since an input has to be stable for three rising clock edges, the encoder pulse width (t_E - low or high) has to be greater than three clock periods ($3t_{CLK}$). This guarantees that the asynchronous input will be stable during three consecutive rising clock edges. A realistic design also has to take

into account finite rise times of the waveforms, asymmetry of the waveforms, and noise. In the presence of large amounts of noise, t_E should be much greater than $3t_{CLK}$ to allow for the interruption of the consecutive level sampling by the three-bit delay filter. It should be noted that a change on the inputs that is qualified by the filter will internally propagate in a maximum of seven clock periods.

The quadrature decoder circuitry imposes a second timing constraint between the external clock and the input signals. There must be at least one clock period between consecutive quadrature states. As shown in Figure 9, a quadrature state is defined by consecutive edges on both channels. Therefore, t_{ES} (encoder state period) > t_{CLK}. The designer must account for deviations from the nominal 90 degree phasing of input signals to guarantee that $t_{ES} > t_{CLK}$.



CHA	CHB	STATE
1	0	1
1	1	2
0	1	3
0	0	4

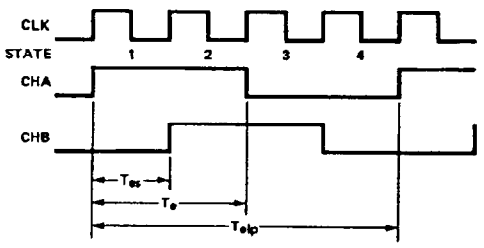


Figure 9. 4x Quadrature Decoding.

Position Counter

This section consists of a 12-bit (HCTL-2000) or 16-bit (HCTL-2016/2020) binary up/down counter which counts on rising clock edges as explained in the Quadrature Decoder Section. All 12 or 16 bits of data are passed to the position data latch. The system can use this count data in several ways:

A. System total range is ≤ 12 or 16 bits, so the count represents "absolute" position.

B. The system is cyclic with ≤ 12 or 16 bits of count per cycle. $\overline{RST}$ is used to reset the counter every cycle and the system uses the data to interpolate within the cycle.

C. System count is > 8, 12, or 16 bits, so the count data is used as a relative or incremental position input for a system software computation of absolute position. In this case counter rollover occurs. In order to prevent loss of position information, the processor must read the outputs of the IC before the count increments one-half of the maximum count capability (i.e. 127. 2047, or 32,767 quadrature counts). Two's-complement arithmetic is normally used to compute position from these periodic position updates. Three modes can be used:
   1. The IC can be put in 8-bit mode by tying the SEL line high, thus simplifying IC interface. The outputs must then be read at least once every 127 quadrature counts.
   2. The HCTL-2000 can be used in 12-bit mode and sampled at least once every 2047 quadrature counts.
   3. The HCTL-2016 or 2020 can be used in 16-bit mode and sampled at least once every 32,767 quadrature counts.

D. The system count is > 16 bits so the HCTL-2020 can be cascaded with other standard counter ICs to give absolute position.

Position Data Latch

The position data latch is a 12/16-bit latch which captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic section during two-byte read operations. The output data is passed to the bus interface section. When active, a signal from the inhibit logic section prevents new data from being captured by the latch, keeping the data stable while successive reads are made through the bus section. The latch is automatically reenabled at the end of these reads. The latch is cleared to 0 asynchronously by the $\overline{RST}$ signal.